AMENDMENTS TO THE CLAIMS

Claims 1-22 (Cancelled)

23. (Currently Amended) A semiconductor device comprising:

a die having:

~~a semiconductor structure that includes a substrate and a plurality of conductive regions formed in the substrate; and~~

~~an interconnect structure having a top surface, and a bottom surface that contacts the semiconductor structure, the interconnect structure having:~~

~~a dielectric structure,~~

~~a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and~~

a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate; and

an interconnect structure connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a dielectric structure, a first metal region that contacts the dielectric structure, and a second metal region that contacts the dielectric structure; and

a test structure including:

a first conductive region having a first surface ~~adhered~~ connected to an exterior surface of the interconnect structure and an opposing second surface;

an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and

a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the

second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

24. (Cancelled)

25. (Currently Amended) The semiconductor device of claim 23 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to ~~a first region on a metal interconnect~~ the first metal region;

a first conductive structure formed in the first opening to ~~make an electrical connection with the first region, and on the top surface to make an electrical connection with~~ electrically connect the first metal region and the first conductive region of the test structure;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to ~~a second region on the metal interconnect~~ the second metal region; and

a second conductive structure formed in the second opening to ~~make an electrical connection with the second region, and on the top surface to make an electrical connection with~~ electrically connect the second metal region and the second conductive region of the test structure.

Claims 26-27 (Cancelled)

28. (Currently Amended) A semiconductor device comprising:

a die having:

~~a semiconductor structure that includes a substrate and a plurality of conductive regions formed in the substrate; and~~

~~an interconnect structure having a top surface, and a bottom surface that contacts the semiconductor structure, the interconnect structure having:~~

~~a dielectric structure,~~

~~a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and~~

a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate; and

an interconnect structure connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a dielectric structure, and a metal trace that contacts the dielectric structure; and

a test structure that contacts the top surface;

a first opening formed in the dielectric structure, the first opening extending from the top surface down to a first region ~~on a metal interconnect~~ of the metal trace;

a first conductive structure formed in the first opening to ~~make an electrical connection with the first region, and on the top surface to make an electrical connection with~~ electrically connect the first region of the metal trace and the test structure;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second region ~~on the metal interconnect~~ of the metal trace;

a second conductive structure formed in the second opening to ~~make an electrical connection with the second region, and on the top surface to make an electrical connection with~~ electrically connect the second region of the metal trace and the test structure; and

a third opening formed in the dielectric structure, the third opening extending from the top surface down through the metal ~~interconnect~~ trace to break an electrical connection between the first and second regions of the metal ~~interconnect~~ trace.

Claims 29-34 (Cancelled)

35. (Previously Presented) The semiconductor device of claim 28 wherein the test device includes a first conductive region having a first surface adhered to an exterior surface of the interconnect structure and an opposing second surface.

36. (Previously Presented) The semiconductor device of claim 35 wherein the test device includes an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region.

37. (Previously Presented) The semiconductor device of claim 36 wherein the test device includes a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

38. (New) A semiconductor device comprising:

a die having:

a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate; and

an interconnect structure connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a number of bond pads, a dielectric structure that contacts the bond pads, a first metal region that contacts the dielectric structure, and a second metal region that contacts the dielectric structure; and

a region of silicon having a bottom surface connected to only a non-conductive region of the top surface of the interconnect structure, and being spaced apart from the bond pads.

39. (New) The semiconductor device of claim 38 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to the first metal region; and

a first conductive structure formed in the first opening, the first conductive structure being electrically connected to the first metal region and the region of silicon.

40. (New) The semiconductor device of claim 39 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to the second metal region; and

a second conductive structure formed in the second opening, the second conductive region being electrically connected to the second metal region and the region of silicon, the first and second conductive structures being spaced apart.

41. (New) The semiconductor device of claim 40 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

42. (New) The semiconductor device of claim 39 and further comprising:

a dielectric region formed to contact the region of silicon;

a conductor region formed to contact the dielectric region, the conductor region being electrically isolated from the region of silicon;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to the second metal region; and

a second conductive structure formed in the second opening, the second conductive structure being electrically connected to the second metal region and the region of silicon, the first and second conductive structures being spaced apart.

43. (New) The semiconductor device of claim 42 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

44. (New) The semiconductor device of claim 38 wherein the region of silicon has a concentration of dopant atoms.

45. (New) The semiconductor device of claim 44 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to the first metal region; and

a first conductive structure formed in the first opening, the first conductive structure being electrically connected to the first metal region and the region of silicon.

46. (New) The semiconductor device of claim 45 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to the second metal region; and

a second conductive structure formed in the second opening, the second conductive structure being electrically connected to the second metal region and the region of silicon, the first and second conductive structures being spaced apart.

47. (New) The semiconductor device of claim 46 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

48. (New) The semiconductor device of claim 44 and further comprising:

a dielectric region formed to contact the region of silicon; and

a conductor region formed to contact the dielectric region, the conductor region being electrically isolated from the region of silicon.

49. (New) The semiconductor device of claim 48 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second metal region; and

a second conductive structure formed in the second opening, the second conductive structure being electrically connected to the second metal region and the conductor region, the first and second conductive structures being spaced apart.

50. (New) The semiconductor device of claim 49 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

51. (New) The semiconductor device of claim 23 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to the first metal region; and

a first conductive structure formed in the first opening, the first conductive structure being electrically connected to the first metal region and the first conductive region.